

Serial No. 09/648,044
Docket No. MIO 0054 PA

Remarks

In the latest Office Action, the Examiner finally rejected claim 45 under 35 U.S.C. 102(e) as anticipated by Kusunoki et al (US 5,369,297). Claims 1, 3 and 5-7 are finally rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kusunoki et al. Claims 2, 4, 8-9, 46-53 and 55-56 are finally rejected under 35 U.S.C. 103(a) as being unpatentable over Kusunoki et al in view of Akram. Claims 10 and 54 are finally rejected under 35 U.S.C. 103(a) as being unpatentable over Kusunoki et al in view of Admitted Prior Art (APA). Claims 11-12, 14 and 57 are finally rejected under 35 U.S.C. 103(a) as being unpatentable over Kusunoki et al in view of Motoyoshi et al (JP 6-53492). Claim 13 is finally rejected under 35 U.S.C. 103(a) as being unpatentable over Kusunoki et al and Motoyoshi et al, as applied to claim 12, and further in view of Akram. The applicants respectfully traverse these rejections.

After reviewing the newly cited reference, we disagree with the Examiner that Kusunoki et al. anticipate or make obvious (individually or in combination with the other cited art) the recited invention of the claims. In particular, Kusunoki et al. fail to teach or suggest a gate formed on a portion of an oxide layer, where a portion of the oxide layer underneath the gate has an ion concentration higher than a remaining second portion under the gate and all other portions of the oxide not covered by the gate. All the embodiments of Kusunoki et al. having a single nitrided oxide portion, which is indicated by symbol 5 in FIGS. 1, 7, 12, 18, and 22, have the gate on the entire oxide layer, and not on a portion thereof. There is no suggestion to the contrary provided by Kusunoki et al.

Independent claim 1 recites the limitation, *inter alia*, "a gate structure formed on a portion of said oxide layer." Independent claim 3 recites the limitation, *inter alia*, "a gate electrode located on said gate oxide layer above said channel region, wherein portions of said gate oxide layer located only under said gate electrode include a first overlap region and a second overlap region, said first overlap region is inward of said source region and adjacent said drain region, said second overlap region includes all remaining portions of said gate oxide layer under said gate electrode and has first and second sides, said first side is adjacent said source region and said second side is adjacent said first overlap region, said first overlap region having an ion implant concentration higher than in said second overlap region and all remaining portions of

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said oxide layer extending outwardly from both sides of the gate electrode, which is effective to lower the surface electrical field in said overlap region." (Emphasis added). Independent claim 12 recites the limitation, *inter alia*, "a gate electrode located on said gate oxide layer above said channel region, wherein portions of said gate oxide layer located only under said gate electrode include a first overlap region and a second overlap region, said first overlap region is inward of said source region and adjacent said drain region, said second overlap region includes all remaining portions of said gate oxide layer under said gate electrode and has first and second sides, said first side is adjacent said first overlap region and said second side is adjacent said source region, said first overlap region having an ion implant concentration higher than in said second overlap region and all remaining portions of said gate oxide layer extending outwardly from both sides of the gate electrode, which is effective to lower the surface electrical field in said overlap region." (Emphasis added). Independent claim 45 recites the limitation, *inter alia*, "a gate electrode located on a portion of said gate oxide layer above said channel region, wherein the portion of said gate oxide layer located only beneath said gate electrode has first and second portions, said first portion is adjacent said drain region, said second portion comprises all remaining portions of said gate oxide layer located under said gate electrode and has first and second sides, said first side is adjacent said first portion and said second side is adjacent said source region, and said first portion has a higher ion implant concentration than in said second portion and all remaining portions of said gate oxide layer extending outwardly from both sides of said gate electrode." (Emphasis added). Independent claim 47 recites the limitation, *inter alia*, "a gate electrode located on said gate oxide layer above said channel region, wherein portions of said gate oxide layer located only beneath said gate electrode include a first portion and a second portion, said first portion is adjacent a first one of said pair of field isolation regions, said second portion comprises all remaining portions of said gate oxide layer under said gate electrode and has first and second sides, said first side is adjacent said first portion and said second side is adjacent a second one of said pair of field isolation regions, and said first portion has a higher ion implant concentration than in said second portion and all remaining portions of said gate oxide layer between said pair of field isolation regions." (Emphasis added).

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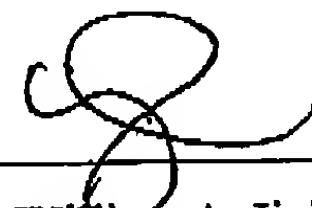
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Accordingly, as Kusunoki et al. does not disclose or even suggest each and every limitation of the claims, the Examiner has failed to establish both anticipation and a *prima facie* case of obviousness.

For all of the above reasons, applicants submit that the pending claims are patentable over the prior art of record and are in condition for allowance. Early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
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